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09/389,048	09/02/1999	KOJI ADACHI	104162	4811

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EXAMINER	
VIDA, MELANIE M	
ART UNIT	**PAPER NUMBER**
2626	

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/389,048	ADACHI ET AL.	
	Examiner	Art Unit	
	Melanie M Vida	2626	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 1999*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-23,29,30 and 33-37* is/are rejected.

7)☒ Claim(s) *5-8,24-28,31 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003 and 15 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is responsive to an amendment, Paper No. 7, filed 8/25/03. Additionally, this action is responsive to a supplementary amendment, Paper No. 8, filed on 9/15/03. Claims 1-37 are pending.

Response to Arguments

2. Applicant's arguments filed Paper No. 7, filed 8/25/03 have been fully considered but they are not persuasive. Applicants alleged support on pages 31-33, and Fig. 8 in the specification for "the later of the M threshold data is less than P" expressed mathematically as (M-S'th)<P. However, the Examiner does not believe that the specification on pages 31 – 33, or Fig. 8 neither quantitatively or qualitatively, supports nor discloses the "later of the M threshold data is less than P". Therefore the 112-2nd rejection is maintained below.

The prior art rejection of Lapstun US Patent No. 6,512,596 is withdrawn because of the applicant's earlier filing date. However, a new ground of rejection is presented below.

Drawings

3. The applicant's are reminded to submit a corrected drawing for figure 2, with an English translation to include the "Prior Art" Label. The Supplementary Amendment filed on 9/15/03 provides corrected drawings with a Japanese to English translation. The Amendment filed on 8/25/03 provides corrected drawings with the "Prior Art" but does not provide an English translation.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claim 21** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. **Claim 21** recites the limitation "the later" in Paper No. 7, page 10, claim 21, lines 9 and 10.

There is insufficient antecedent basis for this limitation in the claim.

7. The specification language in view of **claim 21** is unclear to the Examiner. Specifically, on page 32, lines 9-12, the threshold data 1p or the threshold data 210p in the shift register 2p, does not support the claim language, "the later of the M threshold data pieces is less than P" . Additionally, the threshold data 9p or the threshold data 16p, 17p, to 24p,...,201p to 208p, does not clarify "the later of the M threshold data pieces is less than P" as recited in the claim language (page 32, lines 20-22). Further, the threshold data 209p and 210p in the register 2p are not output to the selectors, or the comparators, and become remaining data as shown at the top state of figure 8, does not support "the later of the M threshold data pieces is less than P" as recited in the claim language (page 32, lines 23 through page 33, lines 1).

Appropriate support in the specification must be clearly indicated with page numbers and the corresponding line numbers, specifically for "the later of the M threshold data pieces is less than P", as recited in the claim language in claim 21.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. **Claims 1-4, 9-13, 16, 21-23, 29-30** are rejected under 35 U.S.C. 102(b) as being anticipated by Fujii et al. US Patent No. 5,781,308 (hereinafter, Fujii).

Regarding, **claim 1,** Fujii teaches a system (60) as shown in figure 6, which reads on a "halftone generation system" that converts a source image comprising plural grey level pixel values at a first resolution into a binary pixel destination image at a second resolution, which reads on "for generating halftone data of a pixel", (col. 4, lines 58-65). The control parameters comprise a threshold matrix (70) that includes plural rows of threshold grey level pixel values which determine a scaled source image will be converted to a white or black dot in the destination image, which reads on "based on comparison between a multilevel image data of the pixel and threshold matrix data", (col. 5, lines 13-18). A SDRAM (86) (static random access memory) stores a threshold matrix in one of the partitioned areas (90), which reads on "threshold matrix data storage means for storing threshold matrix data", (col. 5, lines 59-64; col. 6, lines 16-20).

The controller (100) which reads on "threshold data read means" controls the dither module (96) and state machine (98) to enable synchronous operation when threshold matrix data are loaded into registers, which reads on "for reading all threshold data" applied to grey scale source image

data (88), which reads on "applied to halftone data generation processing for one scanning line from said threshold matrix data storage means", (col. 6, lines 3-11). The threshold register (222), as shown in figures 12 and 14, which reads on "first register means" retains all the threshold values before inputting them into comparator (206), which reads on "for retaining all the read threshold data applied to halftone data generation processing for one scanning line", (col. 10, lines 8-14). Threshold alignment switches (216, 218), as shown in figure 14, accepts mode inputs from a controller (100), which reads on "threshold data selection means", to switch the threshold inputs in response to the modes, which reads on "for selecting a plurality of threshold data pieces from among all the threshold data pieces applied to halftone data generation processing for the scanning line retained in said first register means and outputting the selected threshold data pieces;", (col. 10, lines 45-48). The four comparators (206) as shown in figure 12, which reads on "plurality of comparison means" compare the threshold matrix pixel values with the scaled source image pixels from register (208), which reads on "for performing comparison processing between the threshold data pieces selected by said threshold data selection means and multilevel image data of a plurality of pixels and executing parallel generation processing of halftone data of the pixels", (col. 9, lines 34-37; col. 10, lines 55-57; col. 11, lines 51-60).

Regarding, **claim 2,** please refer to the corresponding rejection in claim 1.

Regarding, **claim 3,** Fujii teaches the threshold align switch (218), which reads on "second register means" that aligns the threshold data corresponding to the scaled image source data (208), which reads on "for retaining all threshold data applied to halftone generation processing for the scanning line to be processed", (col. 10, lines 6-14). The alignment operation of the threshold data within the two pipeline registers (216), (218) corresponding with the scaled

image source data (208) are processed in parallel while the comparators (206) are comparing the previous scaled image source data (208) with the previous threshold data output from the register (218), which reads on "next to the current scanning line where halftone data generation processing is being executed," (col. 9, lines 24-37; col. 10, lines 6-14). For example, as shown in figure 14, during clock cycle 2, threshold values E,A,B,C are read from SRAM (204) under the control of a controller (100) into a threshold pipeline register (220), while threshold values A,B,C,D are transferred from threshold pipeline register (220) into a pipeline register (222), which reads on "said threshold data read means reads all threshold data applied to halftone data generation processing for the scanning line to be processed next to the current scanning line from said threshold matrix data storage means, and outputs the read threshold data to said second register means, and the threshold data retained in said second register means is output to said first register means." The threshold data (A, B, C, D) in clock cycle 2, which reads on "the threshold data retained in said second register means" is output to the threshold pipeline register (222), which reads on "is output to said first register means".

Regarding, **claim 4,** Fujii illustrates in figure 14, during clock cycle 3, the threshold values in SRAM (204) are read into a threshold pipeline register (220), and into the pipeline register (222), which reads on "the parallel generation of halftone data of the pixels in said plurality of comparison means and the reading of all threshold data applied to halftone data generation processing for the scanning line to be processed next to the current scanning line from said threshold matrix data storage means", (col. 10, lines 51-57). Further, the method using the circuitry of figures 12, and 14, Fujii teaches that the alignment and tiling of threshold matrix pixel values simultaneously and in lock step with applied clock signals, which reads on "and the

output processing of the read threshold data to said second register means in said threshold data read means are performed in parallel, (col. 9, lines 30-33).

Regarding, **claim 9,** Fujii teaches as shown in figure 14, that during a mode=0, which reads on "said threshold data read means outputs a shift signal" the threshold data A, B, C, D, read from SRAM (204), is shifted over in clock cycle 2, which reads on "for specifying a threshold data shift amount for said second register means". Fujii teaches that during clock cycles 1 and 2, the controller (100) applies mode=0 to threshold align switches (216) and (218), to result in a straight-through pipelining of threshold matrix pixel values occur from the SRAM into threshold register (220), as shown in figure 14, which reads on "the shift signal indicates the shift amount for causing a start position of a painting object and a threshold data storage location to match ", (col. 10, lines 58-64).

Regarding, **claim 10,** please refer to the corresponding rejection in claim 9.

Regarding, **claim 11,** please refer to the corresponding rejection in claims 1, and 9.

Regarding, **claim 12,** Fujii teaches the alignment function in response to the scaled image source pixels and the mode signal to align with the number of threshold values, which reads on "said threshold read means controls the number of threshold pieces to be read from said threshold matrix data storage means in response to the number of pixels of a painting object on a scanning line to which processing is applied, (col. 10, lines 1-14).

Regarding, **claims 13 and 20,** the controller reads out the threshold values from SRAM into register (220), which reads on "said threshold data read means reads a plurality of threshold data pieces at the same time from said threshold matrix data storage means", (col. 10, lines 61-64).

Regarding, **claims 14-15, and 18-19, 29-30** please refer to the corresponding rejection in claim 1.

Regarding, **claim 16,** please refer to the corresponding rejection in claim 4.

Regarding, **claims 17, and 21,** please refer to the corresponding rejection in claim 3.

Regarding, **claim 22,** Fujii illustrates in figure 14, that certain threshold data pieces are selected in response to a mode triggered by the controller (100), which reads on "said threshold data selection means selects or sorts all threshold data applied to the scanning line read by said threshold data read means in an arbitrary order responsive to the pixel position of generated halftone and outputs the threshold data", (col. 10, lines 61-64).

Regarding, **claim 23,** please refer to the corresponding rejection in claim 4.

10. A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. **Claims 33-34** are rejected under 35 U.S.C. 102(b) as being anticipated by Kato et al. US Patent No. 4,414,581, (hereinafter, Kato).

Regarding, **claim 33,** Kato teaches a dither process implemented with the system shown in figures 1-2, which reads on "a halftone generation system", (col. 5, lines 8-13). The image identification process circuit (4) identifies a type of image from a scanline as belonging to a category comprising photographs and pictures or another category comprising characters and linetone images, which reads on "for simultaneously generating halftone data of a plurality of pixels for each painting object of text and graphics", (col. 2, lines 34-52). Further, a programmable read-only memory (PROM) stores basic dither patterns (50) (51), as shown in figure 4, according to each picture category and for the character category, which reads on "data

storage means for storing binary matrix data pieces equal in number to the tone values formed by binarizing all the tone values of a painting object to be processed", (col. 2, lines 59-65). Additionally, the addressing circuit (5), which reads on "data reading means" designates an address of a threshold in the dither pattern at a two-dimensional position (l, m) based on information from the image identification process circuit (4), which reads on "for selecting binary matrix data of a plurality of pixels from the binary matrix data read out of said data reading means in accordance with main-scanning direction pixel position information of a painting object under processing", (col. 2, lines 64-67). The binary digitizing circuit (7) converts the image signals into binary signals through comparison with the threshold values supplied from the threshold value designating circuit (6), which reads on "outputting the resultant", (col. 3, lines 18-22).

Regarding, **claim 34,** please refer to the corresponding rejection in claim 33.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. **Claims 35-36** rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al. US Patent No. 4,414,581 as applied to claim 33 above, and further in view of Kim, US Patent No. 5,299,030, (hereinafter, Kim).

Regarding, **claim 35,** Kato teaches the halftone generation system of claim 33 above, but fails to expressly disclose that the data read means simultaneously read out all the binary matrix data pieces of a scan line under processing from said data storage means in accordance with a sub-scanning direction pixel position of a painting object under processing.

However, Kim teaches that the image data processed in the sub scan direction (i.e. scan line) of a pixel, the value of m=8, in this case, which reads on "read out all the binary matrix data pieces of a scan line under processing from said data storage means in accordance with a sub-scanning direction pixel position of a painting object under processing", (col. 6, lines 1-5; lines 6-12).

At the time the invention was made it would have been obvious to one of ordinary skill in the art to modify Kato's halftone generation system with Kim's data reading means.

One of ordinary skill in the art would have been motivated to use Kim's data reading means in order to repeat a binarization process in the sub-scan direction, given the express suggestion of Kim, (col. 6, lines 9-10).

Regarding, **claim 36,** Kato teaches the halftone generation system of claim 33 above, but fails to expressly disclose the data reading means reads out the binary matrix data pieces of a scan line under processing from said data storage means in accordance with a main-scanning and sub-scanning direction pixel position information of a painting object under processing.

However, Kim teaches that the dimension of the dither matrix is 8x8, and that an address generator (34) has a means to select the dither matrix repeatedly with the dimension (lxm) of the designated matrix for a window mode select signal to determine a process with simple binarization or with pseudo intermediate tone,, as shown in figure 1, which reads on "the data

reading means reads out the binary matrix data pieces of a scan line under processing from said data storage means in accordance with a main-scanning and sub-scanning direction pixel position information of a painting object under processing", (col. 6, lines 6-7; lines 24-26; col. 7, lines 10-13).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Kato's halftone generation system with Kim's data reading means.

One of ordinary skill in the art would have been motivated to use a data reading means and a data storage means in accordance with a main-scanning and sub-scanning direction pixel in order to binarize a photograph area differently from a character or line area, given the express suggestion of Kato, (col. 2, lines 5-10; lines 44-51).

14. **Claims 37** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al. US Patent No. 4,414,581 as applied to claim 33 above, and further in view of Shu, US Patent No. 5,594,839, (hereinafter, Shu).

Regarding, **claim 37**, Kato teaches the halftone generation system of claim 33, but fails to expressly disclose, "data select means successively shifts the binary matrix data read out by said data reading means till a halftone data generation process of a scan line under processing ends in execution thereof, in accordance with a shift of a main scanning direction pixel position of the painting object to a main scanning direction pixel position of the binary matrix data".

However, Shu teaches of a line offset of the ROM the address applied to ROM lookup table (738) via line (736) by modulo circuit (730) to coordinate the start-of-line (SOL) from address generator (714) produced by lead (726) at the start of each scan line of input pixel values until the number of rows of the dither array has been processed, such that the threshold values

will be resused, and tiled over the image values, which reads on ""data select means successively shifts the binary matrix data read out by said data reading means till a halftone data generation process of a scan line under processing ends in execution thereof, in accordance with a shift of a main scanning direction pixel position of the painting object to a main scanning direction pixel position of the binary matrix data", (col. 10, lines 49-62).

At the time the invention was made it would have been obvious to one of ordinary skill in the art to modify Kato's halftone generation system with Shu's line offset applied to the ROM lookup table (738) for the SOL for scan line of input pixel values.

One of ordinary skill in the art would have been motivated to cause the dither array threshold values to be tiled over the image values, in order to provide a separation screen which can be quickly and economically generated, given the express suggestion of Shu, (col. 4, lines 31-34).

Allowable Subject Matter

15. **Claims 5-8, 24-28, and 31-32** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. **Claim 5** is allowable because the prior art on record does not teach the selector circuits. **Claims 6-8** are allowed because they depend on claim 5 either directly or indirectly. **Claim 24** is allowable because of the crossbar switch circuit. **Claim 25** is allowable because of the barrel shifter circuit. **Claim 26** is allowable because it depends on the allowable claim 24. **Claims 27-28** are allowable because it depends on the allowable claim

25. **Claim 31** is allowable because of the threshold selection step. **Claim 32** is allowable because of the step of sorting threshold data pieces.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fujii et al. US Patent No. 5,778,158 a state machine with scale and dither.

Rust et al. US Patent No. 5,771,105 see figures 13a-13d.

Lin et al. US Patent No. 6,064,359 a dither matrix with a multi-thresholding unit.

Liu, US Patent No. 5,389,938 a dither circuit with a plurality of comparison means, (see figure 2.

Ancin et al. US Patent No. 6,088,512, a void and cluster dither matrix generation for better half-tone uniformity.

Tanioki US Patent No. 4,698,690 a dither ROM (5) with a comparator (4) circuit, see figure 8.

Kerz, US Patent No. 5,581,372, a method for generating and storing thresholds for halftoning an image.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melanie M Vida whose telephone number is (703) 306-4220. The examiner can normally be reached on 8:30 am 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly A Williams can be reached on (703) 305-4863. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Melanie M Vida
Examiner
Art Unit 2626

MMV
mmv

February 4, 2004

KA Williams
KIMBERLY WILLIAMS
SUPERVISORY PATENT EXAMINER